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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/810,310 | 03/26/2004 | Andrew Martin Mallinson | ESST-02701 | 8000 |

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| EXAMINER | |
|---|---|
| JEANGLAUDE, JEAN BRUNER | |
| **ART UNIT** | **PAPER NUMBER** |
| 2819 | |

DATE MAILED: 02/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/810,310 | MALLINSON, ANDREW MARTIN | |
| | Examiner | Art Unit | |
| | Jean B. Jeanglaude | 2819 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *amendment filed on 1-10-05*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☒ Claim(s) *5-15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendments/Arguments

1. Applicant's arguments with respect to claims 1 - 15 have been considered but are moot in view of the new ground(s) of rejection.

Detailed Action

***Claim Objection***

Claims 5 – 15 are objected.

It is not seen where in the drawings "the third segmented series of resistors" includes a current source.

Also, it is not seen in the drawings where "one set of cascaded current sources provides current to one end of the third segmented resistor" as claimed in claim 12.

***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 - 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rivoir et al. (US Patent Number 5,703,588) in view of Ashe (US Patent Number 5,495,245).

4. Regarding claims 1, 2, 3, Rivoir et al. discloses a segmented digital to analog converter (fig. 6) that comprises an input for receiving an input signal (fig. 6); a first segment (50, fig. 6) configured to receive and convert one set of digital bits of the input signal to an analog signal (fig. 6); a second segment (52, fig. 6) configured to receive

and convert a second set of digital bits of the input signal to an analog signal (fig. 6), the second segment (52, fig. 6) having series of resistors (Rf0,...Rf2-1, fig. 6) configured to receive the second set of digital bits (fig. 6), a first current source (54, fig. 6) connected at one end of the series of resistors (52) and a second current source (55, fig. 6) connected at another end of the series of resistors and an output ($V_{out}$) for outputting an analog signal (fig. 6). Moreover, Rivoir et al. discloses a segmented DAC (fig. 6) wherein the current is transmitted between the first and second current source in a manner that substantially removes error in the transmission of the second set of digital bits (fig. 6)[as noted in the abstract the bias current is adjusted such that the voltage drop across the whole of the second resistor string is equal to the voltage drop across the whole of the second resistor string ... second resistor magnitudes to obtain optimum performance without concern for any adverse nonlinearity effects. In obtaining optimum performance without concern for any adverse nonlinearity effects error is removed in the circuit without disturbing the circuit]. Furthermore, Rivoir et al. discloses a segmented DAC (fig. 6) wherein current is transmitted between the first and second current source in a manner that substantially removes in the transmission of the second set of digital bits without creating a disturbance in the circuit as a whole (fig. 6))[as noted in the abstract the bias current is adjusted such that the voltage drop across the whole of the second resistor string is equal to the voltage drop across the whole of the second resistor string ... second resistor magnitudes to obtain optimum performance without concern for any adverse nonlinearity effects. In obtaining optimum performance without concern for any adverse nonlinearity effects error is removed in the circuit without

disturbing the circuit]. Rivoir et al. does not specifically disclose a segmented digital to analog converter that comprises a third segmented series of resistors having a set of resistors from along which an output can be generated. However, Ashe, in a related art, discloses a segmented digital to analog converter (fig. 3) that comprises a first segment resistor (10) that receives a digital input signal; a second segmented resistor (12) that receives a digital input; and a third segmented resistor (14) in series [resistors Rc1,...,Rc8 are in series when switches Sc1,...,Sc8 are opened and the output voltage can be generated]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Rivoir et al.'s system with that of Ashe in order to provide a voltage scaling DAC that is greatly reduced by segmenting the voltage decrementing resistor string into two separate outer strings and an inner string.

5. Regarding claim 4, Rivoir et al. discloses a segmented digital to analog converter (fig. 6) that comprises; a first segment (50, fig. 6) having a first plurality of resistors and configured to receive and convert one set of digital bits of the input signal to an analog signal (fig. 6); a second segment (52, fig. 6) configured to receive and convert a second set of digital bits of the input signal to an analog signal (fig. 6), the second segment (52, fig. 6) having series of resistors (Rf0,...Rf2-1, fig. 6) configured to receive the second set of digital bits (fig. 6), a first current source (54, fig. 6) connected at one end of the series of resistors (52) and a second current source (55, fig. 6) connected at another end of the series of resistors and an output ($V_{out}$) for outputting an analog signal (fig. 6). Rivoir et al. does not specifically disclose a segmented digital to analog converter that comprises a third segmented series of resistors having a set of resistors from along

which an output can be generated. However, Ashe, in a related art, discloses a segmented digital to analog converter (fig. 3) that comprises a first segment resistor (10) that receives a digital input signal; a second segmented resistor (12) that receives a digital input; and a third segmented resistor (14) in series [resistors Rc1,...,Rc8 are in series when switches Sc1,...,Sc8 are opened and the output voltage can be generated]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Rivoir et al.'s system with that of Ashe in order to provide a voltage scaling DAC that is greatly reduced by segmenting the voltage decrementing resistor string into two separate outer strings and an inner string.

Allowable Subject Matter

6. Claims 4 – 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. This condition will also be met when complying with the above objection.

7. Claims 12 – 14 will be allowable when complying with the above objection.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jean B. Jeanglaude whose telephone number is 571-272-1804. The examiner can normally be reached on Monday - Friday 7:30 A. M. - 5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jean Bruner Jeanglaude
Primary Examiner
February 3, 2005